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## NOTICE OF ALLOWANCE AND FEE(S) DUE

23494

7590

12/31/2009

TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265 EXAMINER

SHENG, TOM V

ART UNIT PAPER NUMBER

2629 DATE MAILED: 12/31/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717.235	11/18/2003	Yasushi Kubota	TI-35414	6910

TITLE OF INVENTION: INTEGRATED CIRCUIT FOR SCAN DRIVING

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	03/31/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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Note: A certificate of mailing can only be used for domestic mailings of the CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address) Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission. 23494 7590 12/31/2009 Certificate of Mailing or Transmission TEXAS INSTRUMENTS INCORPORATED I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below. P O BOX 655474, M/S 3999 DALLAS, TX 75265 (Depositor's name (Signature (Date APPLICATION NO. FIRST NAMED INVENTOR ATTORNEY DOCKET NO. CONFIRMATION NO. FILING DATE 10/717,235 11/18/2003 Yasushi Kubota TI-35414 6910 TITLE OF INVENTION: INTEGRATED CIRCUIT FOR SCAN DRIVING APPLN. TYPE SMALL ENTITY ISSUE FEE DUE PUBLICATION FEE DUE PREV. PAID ISSUE FEE TOTAL FEE(S) DUE DATE DUE nonprovisional NO \$1510 \$300 \$0 \$1810 03/31/2010 **EXAMINER** ART UNIT CLASS-SUBCLASS SHENG, TOM V 2629 345-100000 1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). 2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. or agents OR, alternatively, (2) the name of a single firm (having as a member a ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required. registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type) PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment. (A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY) 4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above) 4a. The following fee(s) are submitted: lssue Fee A check is enclosed. Publication Fee (No small entity discount permitted) Payment by credit card. Form PTO-2038 is attached. The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number \_\_\_\_\_\_ (enclose an extra copy of this fo Advance Order - # of Copies \_ (enclose an extra copy of this form). 5. Change in Entity Status (from status indicated above) a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ■ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2). NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office. Authorized Signature Date Typed or printed name Registration No. This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/717,235	11/18/2003	Yasushi Kubota	TI-35414 6910		
23494 75	590 12/31/2009		EXAM	IINER	
TEXAS INSTRU	MENTS INCORPO	SHENG, TOM V			
P O BOX 655474,			ART UNIT	PAPER NUMBER	
DALLAS, TX 752	65		2629		
			DATE MAILED: 12/31/2009		

## **Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 1536 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 1536 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 (571)-272-4200.

	Application No.	Applicant(s)	
	10/717,235	KUBOTA ET AL.	
Notice of Allowability	Examiner	Art Unit	
	TOM V. SHENG	2629	
The MAILING DATE of this communication apperature All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIOF of the Office or upon petition by the applicant. See 37 CFR 1.313 1. ☑ This communication is responsive to BPAI Decision of 12/2/2	(OR REMAINS) CLOSED or other appropriate comn <b>GHTS</b> . This application is and MPEP 1308.	in this application. If not included nunication will be mailed in due course	
2. ☑ The allowed claim(s) is/are 1,3-10 and 12-15.			
3. Acknowledgment is made of a claim for foreign priority unal All b) ☐ Some* c) ☐ None of the:  1. Certified copies of the priority documents have 2. ☐ Certified copies of the priority documents have 3. ☐ Copies of the certified copies of the priority documents have International Bureau (PCT Rule 17.2(a)).  * Certified copies not received:	been received. been received in Applicat	ion No ed in this national stage application fro	
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONM THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.  4. A SUBSTITUTE OATH OR DECLARATION must be subm	ENT of this application.		
INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.  5. CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.  (a) including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached  1) hereto or 2) to Paper No./Mail Date  (b) including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date  Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).  5. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.			
Attachment(s)  1. ☐ Notice of References Cited (PTO-892)  2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)  3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date  4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. ☐ Interview : Paper No 7. ☑ Examiner' 8. ☐ Examiner' 9. ☐ Other /Richard Hjer		•

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### **EXAMINER'S AMENDMENT**

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with attorney William Kempler on 12/18/09.

The application has been amended as follows:

For claim 1:

An integrated circuit for scan driving being used in sequentially selecting and driving scanning lines in a display, which has said plural scanning lines and plural signal lines arranged crossing each other in a matrix configuration, and which has a pixel arranged at each cross point; in this integrated circuit for scan driving, comprising:

a chip, having plural output pads arranged as a column in a first direction, plural drive circuits for driving said scanning lines to the active state through said output pads, respectively, and plural selection circuits for individually selecting said driver circuits in a line-sequential scanning cycle in an order corresponding to the order of said scanning lines:

the odd-numbered output pads, driver circuits and selection circuits corresponding to odd-numbered scanning lines are all arranged in a first region,

the even-numbered output pads, driver circuits and selection circuits corresponding to the even-numbered scanning lines being all arranged in a second

region adjacent to said first region in said first direction;

said first region, in an order corresponding to the order of said odd-numbered scanning lines, said odd-numbered output pads, driver circuits and selection circuits being arranged as columns in said first direction, respectively, and, at the same time, said output pads, driver circuits and selection circuits corresponding to each of the scanning lines are arranged in the same row in the second direction nearly orthogonal to said first direction;

and, in said second region, in an order corresponding to the order of said evennumbered scanning lines, said even-numbered output pads, driver circuits and selection
circuits are arranged as columns in said first direction, and, at the same time, said
output pads, driver circuits and selection circuits corresponding to each of the scanning
lines being arranged in the same row in said second direction[[.]];

said odd-numbered selection circuits are made of individual flip-flops that overall form the first shift register; the first shift data provided by the frame period is transferred sequentially to the latter-stage flip-flops in synchronization with the first transfer clock signal at a frequency half that of the line-sequential scanning cycle; by means of the output signals of the flip-flops with said first shift data latched in them, the corresponding driver circuits are selected;

said even-numbered selection circuits are made of individual flip-flops that overall form the second shift register; the second shift data provided by frame period is transferred sequentially to the latter-stage flip-flops in synchronization with the second transfer clock signal at a frequency half that of the line- sequential scanning cycle and in

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a phase opposite to that of said first transfer clock signal; and, by means of the output signals of the flip-flops with said second shift data latched in them, the corresponding driver circuits are selected.

For claim 2: Cancel claim.

For claim 3:

The integrated circuit for scan driving as in Claim [[2]]1 wherein said first and second shift registers allow bidirectional transfer of, respectively, said first and second shift data.

For claim 4:

An integrated circuit for scan driving being used in sequentially selecting and driving scanning lines in a display, which has said plural scanning lines and plural signal lines arranged crossing each other in a matrix configuration, and which has a pixel arranged at each cross point; in this integrated circuit for scan driving, comprising:

a chip, having plural output pads arranged as a column in a first direction, plural drive circuits for driving said scanning lines to the active state through said output pads, respectively, and plural selection circuits for individually selecting said driver circuits in a line-sequential scanning cycle in an order corresponding to the order of said scanning lines;

the odd-numbered output pads, driver circuits and selection circuits corresponding to odd-numbered scanning lines are all arranged in a first region, the even-numbered output pads, driver circuits and selection circuits

corresponding to the even-numbered scanning lines being all arranged in a second

region adjacent to said first region in said first direction;

said first region, in an order corresponding to the order of said odd-numbered scanning lines, said odd-numbered output pads, driver circuits and selection circuits being arranged as columns in said first direction, respectively, and, at the same time, said output pads, driver circuits and selection circuits corresponding to each of the scanning lines are arranged in the same row in the second direction nearly orthogonal to said first direction;

in said second region, in an order corresponding to the order of said evennumbered scanning lines, said even-numbered output pads, driver circuits and selection
circuits are arranged as columns in said first direction, and, at the same time, said
output pads, driver circuits and selection circuits corresponding to each of the scanning
lines being arranged in the same row in said second direction;

wherein said integrated circuit includes:

a transfer clock generator that divides the fundamental clock signal that defines the cycle of line-sequential scanning in half,

and a shift data generator that generates said first and second shift data in two consecutive cycles of said fundamental clock signal corresponding to the start pulse that indicates the timing of the start of a frame.

#### For claim 8:

A type of integrated circuit for scan driving for sequentially supplying scan drive signal to the scanning electrodes of a display device; comprising:

a first shift register, which has plural register circuits connected in series, and

which sequentially transfers the first shift data corresponding to a first clock signal,

a first drive section, which has plural driver circuits corresponding to the plural register circuits of said first shift register, respectively, and which has said plural driver circuits output drive signals corresponding to said first shift data outputs from the plural register circuits of said first shift register, respectively,

a second shift register, which has plural register circuits connected in series, and which sequentially transfers the second shift data shifted in phase by half a period of a second clock signal with respect to said first shift data corresponding to the second clock signal with its phase deviated by 180° from said first clock signal,

and a second drive section, which has plural driver circuits corresponding to the plural register circuits of said second shift register, respectively, and which has said plural driver circuits output drive signals corresponding to said second shift data outputs from the plural register circuits of said second shift register, respectively;

said drive signals are output alternately from the various driver circuits of said first drive section and the various driver circuits of said second drive section, corresponding to said first or second shift data[[.]];

wherein said integrated circuit has a signal generator, to which the reference clock signal having a frequency double that of said first and second clock signals as well as a start pulse are input, and which generates said first and second clock signals and said first and second shift data on the base of said reference clock signal and said start pulse.

For claim 11: Cancel claim.

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Please add below new claims.

Claim 14: The integrated circuit for scan driving as in Claim 4 wherein said first direction corresponds to the longitudinal direction of said chip, and said output pads are arranged as a column along one edge extending in the longitudinal direction of said chip.

Claim 15: The integrated circuit for scan driving described in Claim 14 wherein the input pads for input of the desired power source voltage or signal are arranged as a column along the other edge in the longitudinal direction of said chip.

### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TOM V. SHENG whose telephone number is (571)272-7684. The examiner can normally be reached on 9:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. V. S./ Examiner, Art Unit 2629

/Richard Hjerpe/ Supervisory Patent Examiner, Art Unit 2629